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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/567,337	09/11/2006	Johann Heyan	03100278AA	4998

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EXAMINER	
PATTON, PAUL E	

ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
05/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,337	HEYAN ET AL.	
	Examiner	Art Unit	
	Paul E. Patton	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/6/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 4, 6, 7, 9, 10, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Viswanathan et al., (US2003/0128080 A1) Viswanathan.

4. As to claims 1 and 7, Viswanathan discloses and shows (Fig 1 & 2) a multichip module having a main circuit board (220), at least one carrier substrate (140) mounted on the main circuit board and which is in electrical contact with the main circuit board, at least one semiconductor chip (130) on the carrier substrate (100) which is in electrical contact with the carrier substrate (110), wherein the carrier substrate has at least one cavity (160) on a mounting surface to accommodate said at least one semiconductor chip, connecting contacts for associated bumps (124) of said at least one semiconductor chip are provided in said at least one cavity (160), the at least one semiconductor chip being mounted on the connecting contact by using the associated bumps in a flip-chip technique, and the mounting surface (143) of the carrier substrate (140) being applied to a contact surface of the main circuit board (220) and the

mounting surface of the carrier substrate wherein the carrier substrate has many layers with conductor tracks (147) extending transversely through a plurality of layers, and a filling material (122) makes contact with a rear of said at least one semiconductor chip (130) in said at least one cavity without enclosing the connecting contacts and bumps including the steps of letting the at least one semiconductor chip into cavities provided for semiconductor chips on a mounting surface of the carrier substrate, mounting the at least one semiconductor chip by making contact with the bumps of the at least one semiconductor chip to connecting contacts in the cavities using a flip-chip technique; applying a layer of filling material to the contact surface of the main circuit board; and applying the carrier substrate having the mounting surface (143) to the contact surface of the main circuit board (220). (Paragraphs [0019] – [0025]).

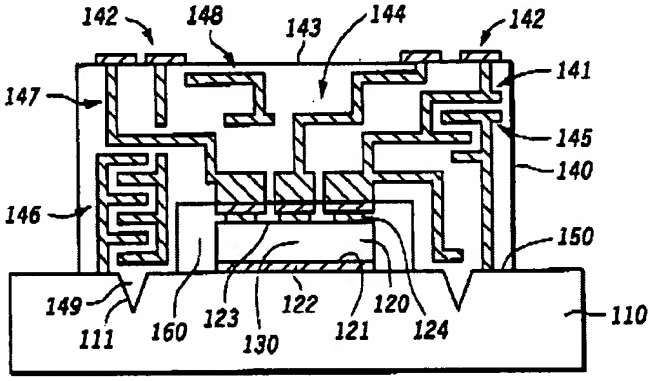

FIG.1

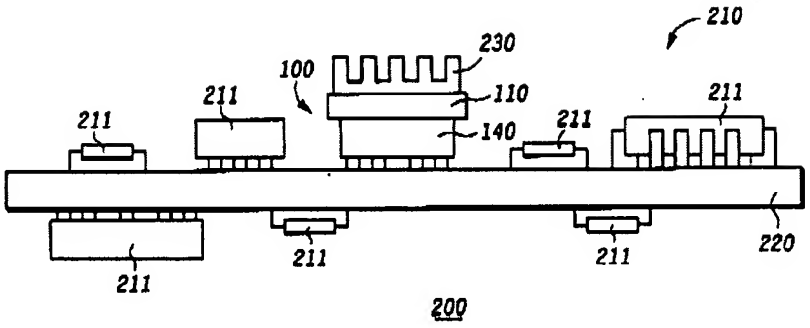

FIG.2

5. As to claims 3 and 9, Viswanathan discloses and shows (Fig 1) that the application of the filling material (122) does not fill the interspaces of the at least one cavity completely.

6. As to claims 4 and 10, Viswanathan discloses and shows (Fig 1 & 2) the conductor tracks (147) of the carrier substrate (140) are led to the mounting surface (143) and are connected electrically and mechanically to conductor tracks of the main circuit board (220) for the simultaneous carrying of signals, dissipation of heat, encapsulation and shielding. (Paragraphs [0021] – [0024]).

7. As to claims 6 and 14, Viswanathan discloses that the carrier substrate is a multilayer, low-temperature co-fired ceramic (LTCC). (Paragraph [0026]).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 8, 12, 13, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viswanathan in view of Takehara et al., (US 2003/0071350 A1) Takehara.

10. As to claims 2, 8, 12, and 15, Viswanathan does not disclose that the filling material is an anisotropically conductive material.

11. Takehara is related to a similar multichip module structure. Takehara discloses that the filler material can be an ACF (anisotropic conductive film) to make the indicated contacts. (Paragraph [0049]).

12. Takehara is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use an anisotropic conductive film as the filler material.

13. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Viswanathan by using an anisotropic conductive film as the filler material for advantages such as reduced interconnect impedance according to the teachings of Takehara. (Paragraph [0051]).

14. As to claims 13 and 16, Viswanathan discloses and shows (Fig 1) that the application of the filling material (122) does not fill the interspaces of the at least one cavity completely.

15. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Viswanathan in view of Yamada et al., (USPAT 6,384,701 B1) Yamada.

16. Viswanathan does not disclose a planar antenna arrangement on an underside of the carrier substrate, which is opposite the mounting surface.

17. Yamada discloses a planar antenna incorporated into a microwave multi-chip module assembly. (Yamada, Column 14, lines 27-30).

18. Yamada is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use a planar antenna arrangement on an underside of the carrier substrate.

19. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Viswanathan by using a planar antenna arrangement on an underside of the carrier substrate for advantages such as providing a small, low-cost microwave device according to the teachings of Yamada. (Column 4, lines 42-47).

20. Claims 11 and 17 - 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viswanathan in view of Nishiguchi, (USPAT 5,064,782) Nishiguchi.

21. Viswanathan does not disclose performing the assembly steps in a gas atmosphere in order to enclose gas in the cavities.

22. Nishiguchi discloses assembling a semiconductor device in a gas atmosphere in order to enclose gas in the cavities. (Nishiguchi, Column 4, lines 13-16).

23. Nishiguchi is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to assemble a semiconductor device in a gas atmosphere in order to enclose gas in the cavities.

24. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Viswanathan by assembling a semiconductor device in a gas atmosphere in order to enclose gas in the cavities for advantages such

as keeping the device in an inert condition according to the teachings of Nishiguchi. (Column 4, lines 16-21).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Patton whose telephone number is 571-272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP

Zandra V. Smith
Supervisory Patent Examiner
30 April 2007

Paul E Patton
Examiner
Art Unit 2822